Timing Kit for 10G-PCIE3-8D Network Adapters

A timing kit is available for CSPi's Myricom 10G-PCIE3-8D network adapters. Myricom network adapters provide timestamps with every packet, even on transmit (a unique feature). The accuracy of these timestamps is very good. Adding the optional timing kit enables connection of even more accurate external oscillators and GPS devices.

An Emerging Legal Requirement

Attaching a GPS offers legally traceable and synchronized time for compliance applications. In Europe, MiFID II introduces a requirement for synchronized, nanosecond resolution timestamps on financial data by 2017. The timing kit is required for MiFID II applications. FINRA in the US requires at least millisecond resolution. The timing kit is optional under FINRA.

Measure Tick-to-Trade Latency while performing Trades

Myricom DBL™ software uses timestamps to measure "tick to trade" latency in nanoseconds. No other low-latency adapter does this.

Accuracy

Using the on-board TCXO, latencies measured at various times in a single day are accurate to 61 bits (ignore the last three bits of the 64-bit value). Connecting an external oscillator through the timing kit can increase this to 62 bits and extend the time elapsed between readings from "single day" to longer periods (better oscillator aging). Connecting a GPS enables mixing timestamps captured on multiple adapters in multiple datacenters.

Automatic Clock Trimming

An FPGA on the Myricom 10G-PCIE3-8D network adapters arithmetically "trims" the onboard clock into synchronization with either on-board or external oscillators. This feature, typically associated with adapters listing for $10,000 or more, is standard on the more competitively priced Myricom adapter.

Enabled by Timing Kit

The optional timing kit allows customers to attach their own GPS and/or atomic clock to the network adapter for the highest accuracies in the industry.

KEY FEATURES

- Adapters without this kit use CSPI's on-board TCXO clock which is significantly better than clocks found on server motherboards

- Connect an OCXO or rubidium 10 MHz clock to remove the short-term jitter from a datacenter's IEEE- 1588 grandmaster signal

- The best latency measurement is acheived with a stand-alone rubidium clock, keeping multiple adapter timestamps synchronized to within ±3 nanoseconds

- Connecting a GPS allows for the comparison of time stamps captured on multiple adapters in multiple datacenters

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Hardware Specifications

KEY SPECIFICATIONS	
Form Factor	The timing kit is a standard height PCI faceplate with two 50 ohm, SMA, female coax connectors attached to ~5.5 inches of coax cable. The coax is terminated with MMCX (microminiature coaxial) connectors that plug into the adapter. Instructions are included for replacing the standard profile faceplate that ships installed onto the adapter. Cables (not supplied) that plug into the timing kit's connectors must terminate in "SMA plugs".
Clock Input	The upper coax connector, marked "CLK", is for an external oscillator. It expects the defacto standard, 10MHz into 50 ohms using a sine wave of 0.5 Vrms (~1.41 Vpp or +7dBm). Although not guaranteed, it should also support a TTL square wave (emitted by some GPS receivers with a 10 MHz clock output) and 75 ohm outputs used by oscillators designed for audio markets. The circuit is transformer isolated. It includes a 1,500 volt Zener diode for protection.
Pulse Input	The lower coax connector, marked "PPS", expects a one pulse-per-second timing reference. The pulse input is directly compatible with 1 PPS signals emitted by most GPS receivers. Specifically, the adapter expects a signal pulse at either TTL levels or at low-voltage TTL levels. The adapter sees a logical zero when voltage levels are below 0.8 volts. It sees a logical one when voltage levels exceed 2.0 volts. The circuit includes a 1,500 volt Zener diode for surge protection. It is opto isolated. The pulse must be of reasonable duration (microseconds to milliseconds).

The pulse input is not directly compatible with some GPS laboratory-grade receivers that expect a high-impedance (500-600 ohms). In that case an external transformer is required. |
Software Support	The APIs for Myricom's DBL™ and Sniffer10G software packages provide timestamps in the metadata associated with each packet. The Linux Ethernet driver provides timestamps via the Linux SO_TIMESTAMPING socket option. The Windows driver does not supply timestamps as there is no Microsoft API for that. However, the alternative UDP/TCP stack that DBL supplies for Windows does support the SO_TIMESTAMPING socket option. The Myricom hardware timestamps are 64-bit numbers with nanosecond resolution.
Support for Switch Timestamps	CSPi's Myricom DBL and Sniffer10G software packages can detect timestamps inserted into packets by Arista switches. If your application is satisfied with the accuracy of the Arista timestamps, the timining kit is not neccessary.
PART NUMBERS	
10G-8D-2SA-SYNC-KIT	Optional front panel kit with timing inputs for the 10G-PCIE3-8D-2S network adapter (Dual SFP+ 10GbE ports on a board with dual QSFP cages shipped with SFP+ adapters).
10G-8D-Q-SYNC-KIT	Optional front panel kit with timing inputs for the 10G-PCIE3-8D-Q network adapter (QSFP configured as four 10GbE ports).
Warranty and add-on support	One year for hardware defects and 90 days for software defects. 90 days of "getting started" telephone and email support as well as any software upgrades shipped within that window. Refer to the support datasheet for options extending the 90- day window.

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